Quantum Transport Properties of Monolayer MoS_2, WS_2, and Black Phosphorus: A Comparative Study

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Abstract

A comparative study of the performance analysis of dual-gate ballistic monolayer Molybdenum disulfide (MoS_2), tungsten disulfide (WS_2), and black phosphorus (BP) field-effect transistors (FETs) is presented. A thorough investigation of output and transfer characteristics infers that WS_2 FET exhibits better performance as compared to MoS_2 and BP. Furthermore, among all three FETs (MoS_2, WS_2, and BP), the WS_2 based FET has a higher carrier velocity. However, variation of gate capacitance (C_G) with gate voltage (V_G) reflects a very good electrostatic gate control of MoS_2 FET due to higher surface charge accumulation. Except for C_G, the overall performance of WS_2 based FET is better than MoS_2 and BP.

Keywords: Transport properties, FET model, Transfer characteristics, Output characteristics.

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Introduction

In 2004 at the University of Manchester, synthesis of the first one atom thick layer of graphene was done by K. S. Novoselove et al. [1-2]. This discovery increases the interest of the scientific community in single-atom-thick two-dimensional (2D) materials to explore their basic properties and applications for device purposes. The absence of energy band gap in the single layer of graphene prevents to manipulate electronic devices made up of graphene [3-5]. A number of different methods are employed for the band gap engineering of graphene, for instance, cutting graphene into one-dimensional strips known as graphene nanoribbons [5-7]. However, these methods add complexity and reduce the charge carrier mobility. As a result of this, the scientific community has focused on other single or few-layered 2D materials. With inherent band gap, transition metal dichalcogenides (TMDs) have overcome the drawbacks of gapless graphene to become a potential material for FET applications in nanoelectronics [8]. Also, they can be easily exfoliated and are stable under vast conditions [9-10].

In the group of materials exhibiting semiconducting nature, TMDs structure is represented by MX_2, where M stands for a transition metal atom (such as Mo or W) and X for a chalcogen atom (such as S, Se, or Te). TMDs feature a multilayer structure with transition metal atoms positioned in the middle of two chalcogen atoms' hexagonal planes. TMDs have an overall hexagonal or rhombohedral symmetry, but the metal atoms inside them

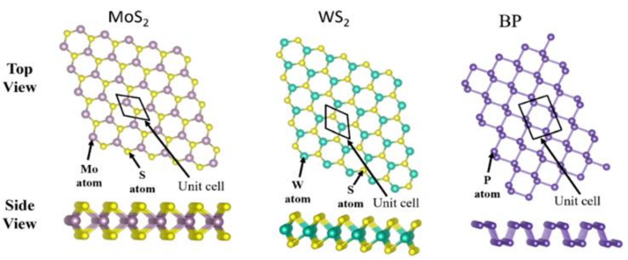

Figure 1: 2D Lattice structures of monolayer MoS_2, WS_2, and BP

display octahedral or trigonal prismatic coordination. According to the literature, MX_2 has a band gap ranging from 1.1 to 2 eV [10]. Therefore, 2D monolayer semiconducting TMDs may be suited for applications that resemble complementary metal oxide-semiconductor (CMOS) logic devices and may be a possible substitute for silicon (Si). Similar to graphene, it is feasible to mechanically exfoliate TMDs' bulk crystals into atomically thin flakes. The exfoliation of 2D TMDs frequently involves electrochemical synthesis, ion intercalation, and mechanical cleavage techniques. Among all the techniques, for mass manufacturing of nanosheets or nanoflakes of layered TMDs, exfoliation via chemicals is most promising [10].

Monolayer MoS_2 has an electron mobility comparable to that of graphene, but with nonzero band gap. The bulk and monolayer forms of MoS_2 have indirect and direct band gaps, respectively. MoS_2 exhibits a transition from 1.3 eV for the bulk indirect band gap to 1.8 eV for the monolayer direct band gap [11]. The reason of this band gap in monolayer MoS_2 is the symmetry breaking of honeycomb lattice [10]. Additionally, monolayer WS_2 with an energy band gap of 1.9 eV is anticipated to have a wide range of applications in energy conversion and renewable energy technologies [12]. Recently, Sebastian *et al.* explored the FET performance of experimentally synthesized monolayers of MoS_2 and WS_2 [13]. Moreover, elemental 2D layered materials such as silicene, phosphorene has been recognized as a new kind of material with unique properties that is critical to the application of electronics and optoelectronics [14]. Monolayer BP (known as "Phosphorene") exhibits a puckered honeycomb structure because each phosphorus atom forms three covalent bonds with its nearest neighbours [15].

In 1914, Bridgman synthesized BP under high pressure and temperature, a brand-new 2D isomer of white phosphorus that is also the most stable allotrope of phosphorus at ambient temperature [16]. BP has received great scientific attention since the successful fabrication of few-layer phosphorene FET in 2014 [15]. BP also exhibits thickness dependent band gap ranging from 0.3 to 2 eV [17]. BP nanosheets, which are more favoured for spectroscopic and electrical studies, have recently been effectively synthesized using liquid-phase exfoliation and chemical vapor de position [18]. 2D lattice structures of monolayer MoS_2, WS_2, and BP are depicted in figure 1. In this work, a comparative study of the ballistic performance of dual-gate monolayer MoS_2, WS_2, and BP FETs is investigated. We have shown the variation of source to drain current density (I_{DS}) against drain voltage (V_D). Also, the gate control performances of monolayer MoS_2, WS_2, and BP FETs are explained by plotting I_{DS} against gate voltage (V_G). Moreover, an explanation of the variation of the average velocity of carriers with V_D and gate capacitance (C_G) with V_G is provided.

Simulation Method & Theoretical Formulation

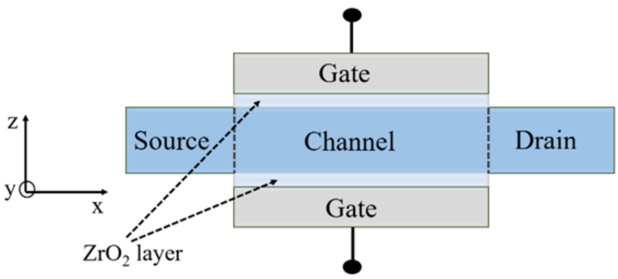

Figure 2: Schematic of ballistic n-type monolayer MoS_2, WS_2, and BP MOSFETs [19].

We have made a comparison between the ballistic performance of monolayer MoS_2, WS_2, and BP channel-based metal-oxide-semiconductor field-effect transistors (MOSFETs). The simulations have been performed on "2DFET" simulation tool [20]. This is a Python simulator for calculating the I-V characteristics of FETs based on 2D materials. The 2D FET channel can be either TMDs or BP. Using this simulator one can model the ballistic limit as well as transport with scattering of both n-type and p-type transistors [20]. The schematic of the structure used for simulation is shown in figure 2. Tables 1 and 2 show the input and control parameters used for simulation in the FET tool, respectively. The theoretical formulation for simulation is described below.

The performance of ballistic MOSFET model can be calculated analytically [21-23]. The equilibrium electron density (n_0) at the top of the energy barrier with zero terminal bias is

$$n_0 = \int_{-\infty}^{\infty} dE\, D(E) f(E - E_F) \qquad \dots (1)$$

where, E represents the energy, D(E) is the density of state at E, f is the Fermi distribution function, and E_F is the Fermi energy. The biasing of the source and drain terminal modulates the energy barriers. Therefore, electrons from the source occupy the positive velocity states at the top of the barrier, while electrons from the drain fill the negative states. The electron density become

$$n = \int_{-\infty}^{\infty} dE\, D\big(E - U_{scf}\big)[f(E - E_{FS}) + f(E - E_{FD})] \dots (2)$$

where E_{FS}, E_{FD} denotes the Fermi level in the source and drain, respectively. U_{scf} denotes the self-consistent surface potential, which is defined as

$$U_{scf} = -\frac{q}{C}(C_G V_G + C_D V_D + C_S V_S) + \frac{q^2}{C}(n - n_0) \dots (3)$$

where C is the sum of the capacitances of the gate (C_G), source (C_S), and drain (C_D), i.e., C = $C_G V_G + C_D V_D + C_S V_S$. The difference between the flux from the source and the drain may be used to determine ballistic current (I_{DS}) once convergence is achieved. Moreover, at the top of the barrier, the average velocity of carriers is given by

$$Average\ velocity = \frac{I_{DS}}{qN} \qquad \dots (4)$$

where q and N represent the electronic charge and density, respectively. For the detailed derivation of the proposed model, one can follow Ref. [24].

Table 1: Parameters taken for the simulation of I_{DS} versus V_D characteristics of FET in ballistic regime.

Gate length	Gate voltage (V_G)	Thickness of insulator (t_{ins})	Dielectric constant of insulator (ε_r)	Drain voltage (V_D)
20 nm	0- 0.6V	3 nm	29 (ZrO_2)	0- 0.6V

Table 2: Control parameters for the device model.

Threshold voltage (V_T)	Gate control parameter (α_G) = C_G/C	Drain control parameter (α_D) = C_D/C	Temperature (T)
0.3 V	0.9	0.03	300 K

Results and Discussion

We have chosen the x-direction along the transistor channel and I_{DS} versus V_D output characteristics of dual gate MOSFETs with high dielectric (ZrO_2) insulator of thickness (t_{ins}) 3 nm is shown in figure 3 (a). It is clear from figure 3 (a) that for an n-type MOSFET, under low bias ($V_G < V_T$), the device is off. Because at low V_G the energy barrier between the source and drain is high, no current flows through the channel. At low V_G, the high value of V_D only lowers the energy of the carriers in the drain contact. However, the high value of V_G reduces the energy barrier, i.e., electron flow from source to drain. For a fixed value of V_G (V_G > V_T), the average velocity of charge carriers increases with the increase of V_D and then saturates. As a result, I_{DS} saturates at high V_D. For low values of V_D, the increase in the I_{DS} linearly varies with an increase in the V_G, i.e., the device behaves as the resistor. Among all three materials (MoS_2, WS_2, and BP), within the ballistic regime, output performance of WS_2 transistor is best.

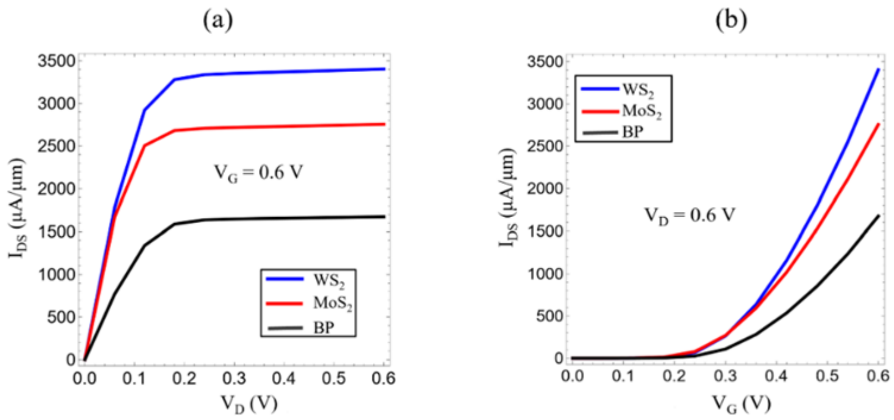

Figure 3: Comparison of output characteristics of n-type monolayer MoS_2, WS_2, and BP FETs. (a) I_{DS} versus V_D at maximum V_G = 0.6 V. (b) I_{DS} versus V_G at maximum V_D = 0.6 V.

We increase the V_G ranging from 0 to 0.6 V in the steps of approximately 0.06 V. As shown in figure 3 (b), for all FETs when $V_G > V_T$, I_{DS} increases with V_G. Although, for V_D = 0.6V, WS_2 has high value of I_{DS} among all the FETs but all three FETs exhibit same value of ON-current. Moreover, except BP, MoS_2 and WS_2 show good gate electrostatic control and high values of I_{DS}. Therefore, for future FETs, monolayer WS_2 and MoS_2 demonstrate huge potential to replace the silicon channel.

In figure 4 (a), for V_G = 0.6 V, we plotted the average electron velocity versus V_D. We observed that for V_D < 0.2 V, all the materials show linear behaviour of electron velocities with increase in V_D. This happens because with increase in the V_D from 0 to 0.2 V, the source to drain voltage decreases, and it acquires a minimum value for V_D > 0.2 V. Therefore, above 0.2 V, the electrons acquire their maximum average velocity. The different values of average velocities in different materials are attributed to their different electron effective masses. Previous studies show that BP has directional effective mass dependency for the electrons [25]. The lower value of average electron velocity of BP FET is due to the higher effective mass of electron in the chosen direction.

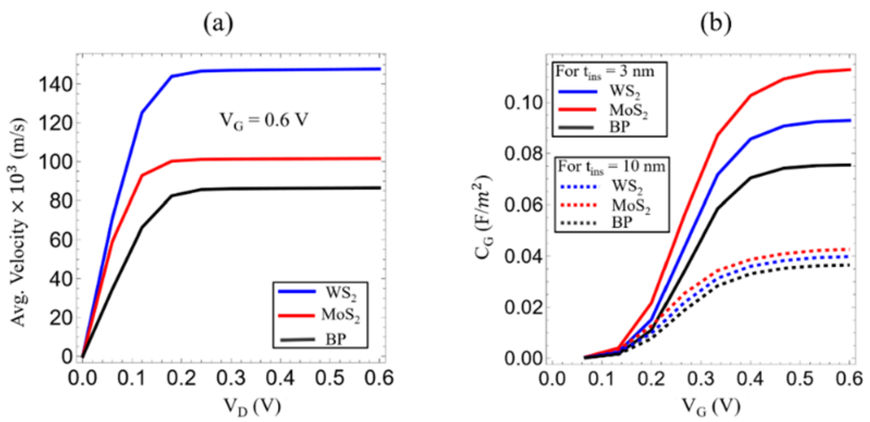

Figure 4: For n-type monolayer MoS_2, WS_2, and BP FETs (a) ballistic transfer characteristics at maximum V_D = 0.6 V and (b) variation of gate C_G with increasing V_G as a function of insulator thickness (tins).

Further, as shown in figure 4 (b), we observe the C_G versus V_G characteristics of the 2D FET with different materials (i.e., MoS_2, WS_2, and BP) and a 3 nm and 10 nm insulating layer. For both 3 nm and 10 nm insulating layers, MoS_2 shows a higher value of C_G than WS_2 and BP. This happens because of the higher dielectric constant of MoS_2 as compared to WS_2 and BP. With a higher V_G, the device is in the accumulation region, and as the V_G decreases, the device comes into the depletion region. Therefore, a reduction in the C_G is observed with a reduction in the V_G. For t_{ins} = 3 nm, higher capacitances are observed for all materials (MoS_2, WS_2, and BP) as compared with t_{ins} = 10 nm because of the inverse dependency of thickness.

Conclusion

In conclusion, we observe that the output characteristics (I_{DS} versus V_D) of n-type MoS_2, WS_2, and BP FETs follow the same trend. For $V_G > V_T$, WS_2 FET has a higher I_{DS} as compared to MoS_2 and BP. Transfer characteristics (I_{DS} versus V_G) show approximately the same value ($\approx$ 0.2 V) of ON-current for all FETs with different values of maximum current. Also, for V_G = 0.6 V, WS_2 FET has higher average carrier velocity when plotted V_D. The higher average velocity is due to the lower effective mass of carriers in WS_2 than MoS_2 and BP. Moreover, the higher value of C_G for MoS_2 FET is due to higher surface charge accumulation as compared to WS_2 and BP based FETs. Therefore, except for C_G, WS_2 FET has better performance.

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